Programme	**:**	**Diploma in ET**/CE/EE//ME/MT/CM/IT/DDGM
Programme Code	**:**	01/02/**03**/04/05/06/07/08/16/**17**/21/22/**23**/24/26
Name of Course	**:**	**Very Large Scale Integration(VLSI)**
Course Code	**:**	**ET 585**

Teaching Scheme:

	Hours /Week	**Total Hours**
Theory	**04**	**64**
Practical	**02**	**32**

Evaluation Scheme:

	Progressive Assessment	**Semester End Examination**			
		Theory	**Practical**	**Oral**	**Term work**
Duration	**Two class tests, each of 60 minutes**	**3 Hrs.**	**3 Hrs.**	**3 Hrs. For batch of 20 students**	**--**
Marks	**20**	**80**	**--**	**25**	**25**

Course Rationale:

The influence of integrated-circuit technology in the past few years on our society has been pervasive, in area ranging from consumer products to business management to manufacturing control. The driving force behind this pervasiveness is that the functional capability of modern integrated circuitry has increased in scope and complexity exponentially with time over the past 20 years. The designers of modern integrated circuitry have continually endeavored to provide more computational speed with less dissipated electrical power and less circuit board area, while maintaining a low failure rate and an aggressive cost. The complexity and speed is finding ready application for VLSI systems in digital processing. Although silicon MOS-based circuitry will meet most requirements in such systems .The student can acquire knowledge in the design skill of combinational and sequential circuit with the help of VHDL and CMOS Logic circuit processing operation, student can use this knowledge as technician, supervisor and programmer in different sections of industry.

Course Objectives:

After studying this course, the student will be able to

•	Develop the state diagram, state table
•	Develop model of Moore and Mealy machine
•	Implement CMOS logic and logical equations.
•	Comprehend CMOS processing Technology
•	Comprehend Hardware description language , its components and programming syntax
•	Develop program to implement combinational and sequential logic circuit using VHDL
•	Comprehend VHDL simulation and synthesis
•	Comprehend ASIC, FPGA and PLDs.

Course Content:

Chapter No.	Name of Topic/Sub topic	Hrs	Marks
	SECTION – I		
1.	**Introduction**		
	1.1. Review of Sequential Logic : Asynchronous and Synchronous, Metastability, Noise margins, Power Fan-out, Skew (Definitions only) 1.2. Moore and Mealy Models, state machine notation, examples on Moore and mealy: counter, sequence detector only	8	12
2.	**VLSI Design Concepts and Technology**		
	2.1 Comparison of BJT and CMOS parameters 2.2 Design of Basic gates using CMOS: Inverter, NOR,NAND, MOS transistor switches, transmission gates. 2.3 Drawing of complex logic using CMOS (building of logic gate as per the Boolean equation of three variable) 2.4 Estimation of layout resistance and capacitance, switching characteristics, 2.5 Fabrication process: Overview of wafer processing,Oxidation, epitaxy, deposition, Ion–Implementation and diffusion, silicon gate process. 2.6 Basics of NMOS, PMOS and CMOS: nwell, pwell, twin tub process.	13	12
3.	**Introduction:Hardware Description Language (HDL)**		
	3.1 Introduction to HDL: History of VHDL, Pro's and Con's of VHDL 3.2 VHDL Flow elements of VHDL(Entity, Architecture,configuration, package, library only definitions) 3.3 Data Types, operators, operations 3.4 Signal, constant and variables(syntax and use)	12	16
	SECTION – II		
4.	**Hardware Description Language (HDL)**		
	4.1 Concurrent constructs (when, with, process) 4.2 Sequential Constructs (process, if, case, loop, assert, wait) 4.3 Simple VHDL program to implement Flip Flop, Counter, 4.4 shift register, MUX, DEMUX, ENCODER, DECODER 4.5 MOORE, MEALY machines 4.6Test bench and its applications	12	16
5	**Simulation and Synthesis**		
	5.1 Event scheduling, sensitivity list, zero modeling, simulation cycle 5.2 Comparison of software and hardware description language,delta delay 5.3 Types of simulator event based and cycle based . 5.4 HDL Design flow for synthesis 5.5 Efficient Coding Styles, Optimizing arithmetic expression,sharing of complex operator	13	12

6.	**Architecture of ASIC and PLD**		
	6.1 ASIC design flow 6.2 CPLD -Xilinx and Atmel series architecture, Details of internal block diagram 6.3 Introduction to FPGA like Xilinx (FPGA), SPARTAN 3 series and Atmel	06	12
	TOTAL	64	80

List of Practical/Experiments/Assignments:

Sr. No.	Name of Experiment/Assignment	Hrs
1.	Write VHDL program for any two basic gates.	02
2.	Write VHDL program for full adder / subtractor & Synthesize using FPGA	04
3.	Write VHDL program for 8:1 multiplexer & Synthesize using FPGA	02
4	Write VHDL program for 2:4 Decoder & Synthesize using FPGA	02
5.	Write VHDL program for 8:3 Encoder & Synthesize using FPGA	02
6.	Write VHDL program for synchronous counter & Synthesize using FPGA	04
7.	Write VHDL program for binary to gray code converter & synthesize using FPGA	02
8.	Write VHDL program for RS,JK, FLIPFLOP & Synthesize using FPGA	04
9	Write VHDL program for D ,T FLIPFLOP & Synthesize using FPGA	02
10.	Write VHDL program for SHIFT REGISTER& Synthesize using FPGA	04
11.	Implement four Bit ALU or sequence generator.	04
	Total	32

Instructional Strategy:

Sr. No.	Topic	Instructional Strategy
1.	Introduction	Class room teaching
2.	VLSI Design Concepts and Technology	Class room teaching
3.	Introduction:Hardware Description Language (HDL)	Class room teaching and labortary
4.	Hardware Description Language (HDL)	Class room teaching and labortary
5.	Simulation and Synthesis	Class room teaching and labortary
6.	Architecture of ASIC and PLD	Class room teaching

Books:

Sr. No.	Author	Title	Publication
1.	Gaganpreet Kaur	VHDL Basics to programming	Pearson
2	John M. Yarbrough	Digital Logic: Application and design	Thomson
3	William I. Fletcher	An Engineering approach to digital design	Prentice-Hall of India
4	Neil H. E. Weste Kamran Eshraghian	Principals Of CMOS VLSI Design: A Systems Perspective	Pearson Education
5	Douglas Perry	VHDL Programming by example	Tata McGraw-Hill
6	Sarkar & Sarkar	VLSI design and EDA tools	Scitech Publication India Ltd

Specification Table:

Sr. No.	Topic	Cognitive Levels			Total
		Knowledge	Comprehension	Application	
1.	Introduction & Physical layer	06	04	06	16
2.	The Data Link Layer	04	04	04	12
3.	Medium Access Sub layer	04	04	04	12
4.	The Network Layer	04	04	04	12
5.	The Transport Layer	06	04	06	16
6.	The Application Layer	04	04	04	12
	Total	28	24	28	80

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